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(editors)

New Trends in Information Technologies

I T H E A
SOFIA
2010

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ITHEA®

Sofia, Bulgaria, 2010

ISBN 978-954-16-0044-9

First edition

Recommended for publication by The Scientific Concil of the Institute of Information Theories and Applications FOI ITHEA

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It is represented that book articles will be interesting for experts in the field of information technologies as well as for practical users.

General Sponsor: Consortium FOI Bulgaria (www.foibg.com).

Printed in Bulgaria

ISBN 978-954-16-0044-9

C\o Jusautor, Sofia, 2010

LARGE VLSI ARRAYS – POWER AND ARCHITECTURAL PERSPECTIVES

Adam Teman, Orly Yadid-Pecht and Alexander Fish

***Abstract**: A novel approach to power reduction in VLSI arrays is proposed. This approach includes recognition of the similarities in architectures and power profiles of different types of arrays, adaptation of methods developed for one on others and component sharing when several arrays are embedded in the same system and mutually operated. Two types of arrays are discussed: Image Sensor pixel arrays and SRAM bitcell arrays. For both types of arrays, architectures and major sources of power consumption are presented and several examples of power reduction techniques are discussed. Similarities between the architectures and power components of the two types of arrays are displayed. A number of peripheral sharing techniques for systems employing both Image Sensors and SRAM arrays are proposed and discussed. Finally, a practical example of a smart image sensor with an embedded memory is given, using an Adaptive Bulk Biasing Control scheme. The peripheral sharing and power saving techniques used in this system are discussed. This example was implemented in a standard 90nm CMOS process and showed a 26% leakage reduction as compared to standard systems.*

***Keywords**: VLSI Arrays, SRAM, Smart Image Sensors, Low Power, AB²C.*

***ACM Classification Keywords**: B.3.1 Semiconductor Memories - SRAM, B.6 Logic Design – Memory Control and Access, B.7 Integrated Circuits – VLSI, E.1 Data Structures – Arrays, I.4.1 Digitization and Image Capture*

Introduction

The continuing persistence of Moore's Law [Moore65] throughout recent years has led to great opportunities for embedding complex systems and extended functionality on a single die. The primary example of this trend is the modern day, high performance, multi-core microprocessor that employs large memory caches in order to achieve large bandwidth. Another popular example is the smart image sensor, which integrates additional capabilities of analog and digital signal processing into a conventional CMOS sensor array. Both microprocessors and image sensors are frequent components of various Systems-On-Chip (SOC) that also embed several additional SRAM arrays for various functionality. As a result of these trends, large VLSI arrays frequently cover a large area of various microelectronic systems, sometime well over half of the total silicon die.

One of the side effects of the integration of large VLSI arrays is, of course, power consumption. In the last decade, low-power design has ousted high-performance as the main focus of the VLSI industry. This is a result of the constant exponential rise in power density over the past three decades, coupled with the rise in popularity of mobile, battery powered devices. This power increase proved to be unacceptable in immobile, high performance systems, when the cost and complexity of heat dissipation became too high, and in mobile devices, where increased performance and functionality are required alongside the need for large spans between recharging. In today's systems, it is very common that the main source of power consumption is the large memory arrays. In digital camera systems, the pixel array along with its periphery are obviously the main consumers of power, and likewise, in other SOCs comprising smart imagers, they tend to be close to the top of the list. These facts lead us to realization that low power solutions for embedded arrays are a necessity in modern VLSI design.

In this paper, we have chosen the two types of arrays mentioned above, embedded SRAM bitcell arrays and image sensor pixel arrays, for discussion. Through these examples, we will show that there are several similarities in the architectures and power profiles of different types of arrays. Many techniques and solutions have been developed for power reduction in each type of array, but rarely has one technique been adapted to fit

another type of array. Through our discussion, we will show that such possibilities exist and provide an important direction for low power research.

The discussion will start with a review of the architectures of both types of subsystems (i.e. bitcell and pixel arrays), describing the components that compose each. We will then discuss the sources of power consumption and the related problems for each subsystem, as well as a number of existing low power solutions for each case. We will continue with a comparison of the two types of subsystems, highlighting similarities and discussing peripheral sharing opportunities. Finally, we will give an example of a system, recently developed by our group, that utilizes these similarities to achieve power reduction in a smart image sensor system with embedded memory.

SRAM Architecture and Power Considerations

Modern digital systems require the capability of storing and accessing large amounts of information at high speeds. Of the different types of memories, the Static Random Access Memory (SRAM) is the most common embedded memory, due to its high speeds and relatively high density in standard fabrication processes. SRAMs are widely used in microprocessors as caches, tag arrays, register files, branch table predictors, instruction windows, etc. and occupy a significant portion of the die area. In high-performance processors, L1 and L2 caches alone occupy over half of the die area [Mamidipaka, 2004]. Accordingly, SRAMs are one of the main sources of power dissipation in modern VLSI chips, especially high-end microprocessors and SOCs.

Figure 1 shows a typical block diagram of an SRAM, with emphasis on the main components and sub-blocks. The core of the SRAM is an array of identical bitcells, laid out in a very regular and repetitive structure, each bitcell storing either a '1' or '0' on a cross-coupled latch, and enabling read and write access. The bitcells are divided into rows and columns, allowing complete random access, through the use of X and Y addressing circuitry consisting of a row decoder and a column multiplexer. The addressing is propagated to the individual bitcell through a grid of horizontally wired *wordlines* and vertically wired *bitlines*. A particular bitcell is accessed (either read or written) when its row's wordline and its column's bitline are asserted simultaneously.

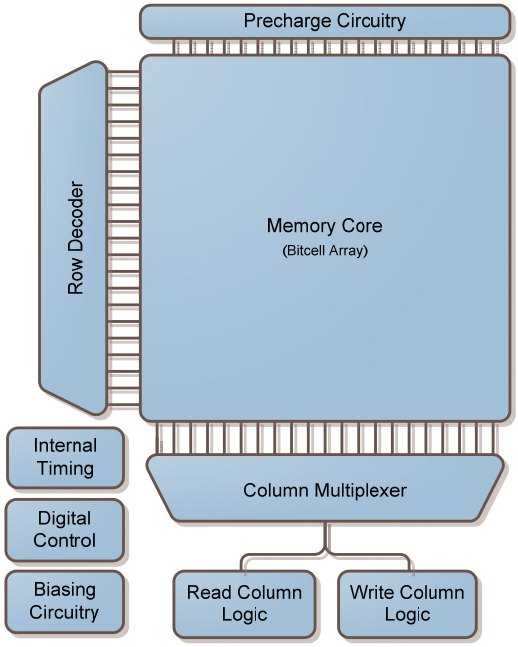

Figure 1: Typical SRAM Component Block Diagram

In order to initiate either a read or a write, the read column logic and write column logic blocks are required. The read column logic block typically consists of a low swing sense amplifier to enhance the performance and readout a digital signal from the asserted column. The write column logic block consists of a write driver that asserts the data to be written onto the relevant column. A read/write enable control signal selects which of the two blocks is activated, and the asserted wordline initiates the bitcell on the selected column to be read from or written to.

Additional blocks needed for SRAM operation include column precharge, internal timing, digital control blocks and biasing circuitry. The column precharge block prepares the read/write operation by setting the columns into a known state. The internal timing blocks sense various transitions in internal and external signals to initiate or terminate operation phases. The digital control blocks enable application of advanced error correcting, row/column redundancy, etc. The biasing circuitry is generally required for sense amplifier operation.

The power profile of SRAMs include both dynamic power, consumed during read and write operations, as well as static power, consumed during standby ("hold") periods. The dynamic power, similar to standard logic, is a function of the supply voltage and frequency, giving the standard tradeoff between power and performance/reliability. Static power in SRAMs, on the other hand, is mainly due to unwanted parasitic leakage currents. As technology scales, leakage currents become a more dominant factor, causing the static power of SRAMs to become a major issue and one of the primary static power components of many systems. A unified active power equation is given in Equation 1 [Rabaey2003] [Itoh2001]:

$$\begin{aligned} P &= V_{DD}\left(I_{array} + I_{decode} + I_{periphery}\right) = \\ &= V_{DD}\left\{\left[m i_{act} + m\left(n-1\right) i_{hld}\right] + \left[\left(n+m\right) C_{DE} V_{\text{int}} f\right] + \left[C_{PT} V_{\text{int}} f + I_{DCP}\right]\right\} \end{aligned} \quad (1)$$

where m and n are the number of columns and rows, respectively, f is the operating frequency, V_{DD} is the general supply voltage, V_{int} is the internal supply voltage, i_{act} is the effective current of the selected cells, i_{hld} is the data retention current of inactive cells, C_{DE} is the output node capacitance of each decoder, C_{PT} is the total capacitance of the digital logic and periphery circuits, and I_{DCP} is the static current of the periphery.

The dynamic power of an SRAM is mainly consumed in the following areas: address decoding, bitline charging/discharging, and readout sensing. During address decoding, power is consumed both by the switching of the decoders themselves, as well as by charging and discharging the selected wordlines, which can have high capacitances. During both read and write operations, the bitlines are precharged and subsequently discharged. This is especially power consuming during writes, when the bitline is fully discharged, or when a full discharge read scheme is chosen. Sense amplifiers typically depend on bias currents for operation, consuming constant power when they are activated.

The static power of an SRAM is primarily consumed through leakage currents inside the bitcells themselves during standby (hold) periods, i.e. when the particular cell (or the whole array) is not asserted. This includes subthreshold and gate leakages in both the inner cross coupled latch structure, as well as to/from the bitlines through the access transistors on unselected rows. Another large contributor to static power is from the precharge circuitry, when a constant charging scheme is used, i.e. a high-resistance supply or diode-connected transistor is placed on the bitlines to replenish lost precharge voltage. Other contributors to the static power are the leakage currents in the decoders and other blocks.

An in-depth analysis of the power dissipation by all SRAM components can be found in [Itoh2001].

Several standard methods have been developed over the years to reduce the power consumption of SRAMs. The standard methods are based on physical partitioning of the array in each of the axes. Banked organization of SRAMs divides the array both horizontally and vertically into sub-arrays. An external decoder raises the chip select of the selected bank, reducing the dynamic power consumption, as smaller decoders are needed, and less

wordline and bitline capacitances are charged/discharged. The Divided Word Line (DWL) approach divides the array horizontally, propagating the decoder output on a global wordline, and subsequently raising the local wordline of a partition of columns, reducing the overall capacitance charged, and requiring smaller wordline drivers. Partitioning the columns using the Divided Bitline scheme, with partial multiplexing inside the array, reduces the bitline capacitance and in certain sensing schemes, will reduce the power consumption. All of these solutions come at the expense of additional area overhead, but a good tradeoff can achieve a worthwhile reduction of power consumption as well as an improvement in performance.

Using advanced timing and sensing schemes is another standard method to achieve a substantial dynamic power reduction. Using pulsed word lines and/or reduced bitline voltage swings, results in less discharge during read cycles, but is accompanied with complex design considerations and higher sensitivity to process variations. Timing the activation of sense amplifiers limits biasing currents to be present only during the exact times that the sensing is carried out. Additional low static power sense amplifiers, such as a Differential Charge Amplifiers and Self Latching Sense Amplifiers, also achieve static power reduction.

Many schemes have been proposed to reduce the bitcell leakage power, such as Supply Voltage Gating [Powell2000] [Flautner2002], Reversed Body Biasing (RBB) [Nii1998] [Hanson2003], Dynamic Voltage Scaling [Kim2002] and Negative Word Line (NWL) application [Wang 2007]. Recently, many proposals have shown minimum energy point operation of SRAMs in the subthreshold or near-subthreshold region. Examples of these include various works by Chandrakasan and Calhoun et.al. [Chandrakasan2007] [Chandrakasan2008] [Calhoun2007].

CMOS Image Sensor Architecture and Power Considerations

Traditionally, digital image sensors were fabricated in Charge Coupled Device (CCD) technology, but the integration of image sensors into more and more products, made the Active Pixel Sensor (APS) an attractive solution. This image sensor architecture is implemented in standard CMOS technology processes, and provides significant advantages over the CCD imagers in terms of power consumption, low voltage operation, and monolithic integration. With the rising popularity of portable, battery operated devices that require high-density ultra low power image sensors, the CMOS alternative has become very widespread. In addition, the CMOS technology allow for the fabrication of so called “smart” image sensors that integrate analog and/or digital signal processing onto the same substrate as the imager and its digital interface. Low power smart image sensors are very useful in a variety of applications, such as space, automotive, medical, security, industrial and others [Fish2007].

CMOS image sensors generally operate in one of two modes: rolling shutter or global shutter (snapshot) mode. When rolling shutter mode is used, each row of pixels is initiated for image capture separately in a serial fashion. This creates a slight delay between adjacent rows, resulting in image distortion in cases of relative motion between the imager and the scene. With the global shutter technique, the image is captured simultaneously by all pixels, after which the exposure is stopped, and the data is stored in-pixel while the image is read out. The operation of both techniques can be divided into three stages: *Reset, Phototransduction and Readout*. During the *Reset* stage, an initial voltage is set on the photodiode capacitance that constitutes most of the pixel area. Subsequently, the pixel enters the *Phototransduction* stage, during which the incident illumination causes the capacitance to discharge throughout a constant integration time. Readout is commenced at the end of the integration time, and the final value of the pixel is read out and converted to a digital value.

Figure 2 shows a component block diagram of a generic smart CMOS APS based image sensor. The core of the image sensor is a pixel array, generally consisting of a photodiode, in-pixel amplification, a selection scheme and a reset scheme. A full description of the operation of this pixel is given by Yadid-Pecht, et.al. [Yadid-Pecht2004].

Some smart imagers employ more complex pixels, enabling them to perform analog image processing at the pixel level, such as A/D conversion.

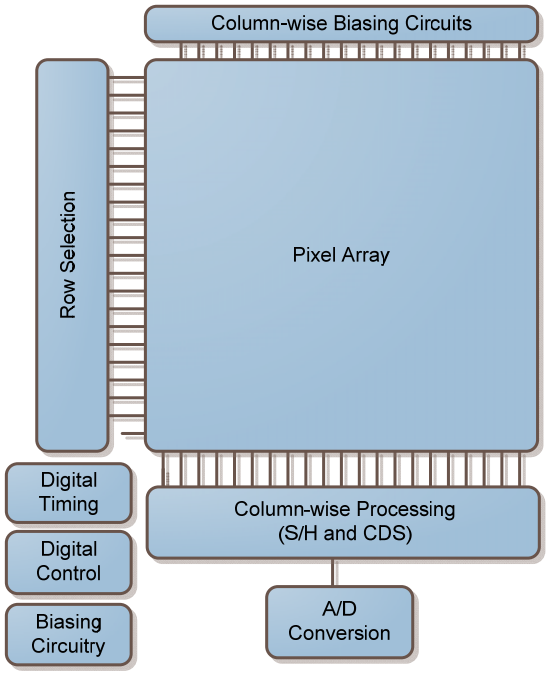

Figure 2: Generic Smart Image Sensor Component Block Diagram

Access to the pixels is carried out through the row selection block. This is usually made up of a shift register, as serial access is commonly employed, although in certain applications, a digital decoder is preferred. An entire row is generally accessed simultaneously for both reset and readout operations, except for in applications where random access is required, such as tracking window systems.

Several blocks are required at every column for the parallel operation of an entire pixel row. These include Sample and Hold (S/H) circuits, Corellated Double Sampling circuits and Analog to Digital Converters (ADC). The S/H circuitry generally measures the reset level of the pixels to enable the CDS to remove Fixed Pattern Noise (FPN). Column-wise ADCs are only one option; the others being in-pixel ADC or single ADC per imager. The selected scheme will be according to the tradeoffs of area, power, speed and precision.

Additional blocks that are required in the periphery of the imager include the general Biasing Circuitry and Bandgap References for creating biasing currents for the in-pixel signal amplifiers, usually implemented through a Source Follower (SF) scheme. and the ADCs; Digital Timing and Digital Control blocks for producing the proper sequencing of the addresses, ADC timing, etc.

The sensitivity of a digital image sensor is usually proportional to the area of the photodiode and the resolution is set by the number of pixels. This results in a relatively large area covered by the image sensor, compared to other on-chip circuits, and accordingly, a large percentage of the overall power consumption. The contribution of different image sensor components to overall power dissipation may vary significantly from system to system. For example, pixel array power dissipation can vary from a number of μWatts for a small array employing 3 transistor APS architecture to hundreds of mWatts for large format "smart" imagers employing in-pixel analog or digital processing. The power dissipation of the pixel array of a generic “smart” image sensor can be given by Equation 2:

$$P_{Array} = F_R \times N \times M \times \left(E_{reset} + E_{read\_out} + E_{ana\log} + E_{digital} \right) + N \times M \times P_{leakage} \quad (2)$$

where F_R is the imager's frame rate, N and M are the number of rows and columns, respectively, E_{reset} is the energy required for pixel reset, E_{read_out} is the energy dissipated during signal readout during one frame, E_{analog} and $E_{digital}$ are energy dissipation components dissipated by in-pixel analog and/or digital processing during one frame and $P_{leakage}$ is the in-pixel leakage power.

The dynamic power in the above equation is proportional to the frame rate and is composed of the energy required to refill the photodiode capacitance during reset; the power dissipated through column-wise biasing currents during readout; and additional energy consumed by (optional) in-pixel functionality. The static power is due to leakage through the reset and row selection switches during integration and standby periods. These leakages also degrade the performance and precision of the imager.

The row selection block can be another major source of power dissipation, depending on the size of the array and the method of operation. In both global and rolling shutter modes, the row reset and row selection capacitances are periodically charged, proportional to the frame rate. In window tracking applications, on the other hand, the power of the row (and column) selection blocks can be dominated by leakage power, as the majority of the rows/columns may not be asserted for long periods.

The other primary source of power dissipation is the analog circuitry, including the ADCs, S/H, CDS and biasing circuitry. Optimally, these are timed to consume power only during their precise periods of operation, but they generally have a high power profile. The analog peripheral blocks present a constant tradeoff between speed, noise immunity, and precision versus power consumption and area, and for low power systems, the choice of these blocks needs to be made cautiously.

Additional power is dissipated in the digital timing and control blocks; however, the complexity and frequency of these tend to be lower than standard digital circuits, and so most common power reduction techniques can be implemented on these blocks.

An in depth description of all the contributions to power dissipation in a smart image sensor is given by Fish, et.al. [Fish2008].

Image sensors provide power reduction opportunities at all the design levels, starting with the technology and device levels, through the circuit level and all the way to the architecture and algorithm level. Standard power reduction techniques, such as supply voltage reduction and technology scaling, aren't always applicable to CMOS image sensors, as they are frequently accompanied by unacceptable tradeoffs. Supply voltage reduction reduces both the precision and the noise immunity of image sensors, while technology scaling generally includes side effects, such as increased leakage current and dark current, as well as reduced photoresponsivity. However, at the technology level, processes can be modified for low power image sensor fabrication albeit, at an increased cost. An example of such a process is the Silicon-on-Sapphire (SOS) process that provides a very low power figure and enables backside illumination [Culuriciello2004].

The device and circuit level provide several opportunities for limiting power dissipation, depending on the options and layers provided by the chosen technology. The presence of separate wells for both nMOS and pMOS transistors enables the application of body biasing on inactive rows for leakage reduction. This technique loses its effect with scaling, as the effect on a devices threshold voltage is reduced, but image sensors are generally fabricated in technologies up to 90nm, where it is still efficient. Additional devices, such as high-VT transistors and thick oxide transistors can also be used for leakage reduction on slow busses. Another technique commonly used for leakage reduction is serial connection of "off" transistors for "stack effect" utilization [Narendra2001].

Smart image sensors provide many interesting opportunities for power reduction at the architectural and algorithm levels. Depending on the functionality of the sensor, these systems can be equipped with designated blocks for eliminating unnecessary power consumption. An example of this is the tracking sensor we proposed

[Teman2008] that used row and column shift registers for window definition and an analog winner-take-all circuit for motion tracking. In this system, the pixels outside the window of interest were deactivated and ADCs were used only for initial detection. The switching activity of the shift registers was very low, as well, further reducing the system power consumption.

Similarities between SRAMs and Image Sensors

In the previous two sections, the architectures and power profiles of two types of VLSI arrays, SRAMs and Image Sensors, were presented along with a number of examples of methods for reducing the power consumption of each. This section will deal with the similarities between these two architectures and their sources of power dissipation, arguing that low power approaches and methods developed for one type of array should be researched and adapted for the other.

Clearly, the first similarity between the two architectures is the two-dimensional array based structure of *m* rows and *n* columns of identical unit cells. SRAM bitcells have been optimized over the years to produce a dense layout to fit as much memory as possible onto a given area. This is possible due to the regular patterning of the cells, allowing many exceptions in design rules. The dense layout results in reduced capacitances, provides benefits in power and performance, as well as smaller peripheral circuits for a given memory size. In the case of pixel arrays, dense layouts provide similar benefits; however, the reduction in pixel size has a negative effect on pixel sensitivity, quantum efficiency, noise figures, etc. Various approaches for an optimal pixel layout have been proposed, such as the hexagonal shaped pixel [Staples2009].

For both SRAM bitcell and imager pixel design, leakage current during idle cycles (“hold” cycles for bitcells and “integration” cycles for pixels) has become a major focus. In some cases, smart image sensors contain memory circuits in-pixel, which further deepens the similarity. Utilization of leakage reduction methods, such as multiple threshold transistors and body biasing have been presented for both types of arrays. Modern CMOS processes include designated transistors for use in SRAM bitcells, optimized for leakage reduction. Several groups are researching low voltage operation of SRAMs in the subthreshold or near-subthreshold regions of operation. This approach could be used for image sensors, especially for operation of in-pixel or peripheral logic, due to their reduced frequency requirements.

Random or pseudo-random access to the unit cells in both types of arrays is achieved through row and column addressing. In SRAM design, the row addressing for wordline assertion is generally achieved through a row decoder, while standard image sensors, operating in the global or rolling shutter modes, use shift registers for reset and row selection. Both types of circuits are fitted to the pitch of the rows for layout and have been deeply researched for optimal operation in terms of power, area and performance, especially due to the fact that they drive large capacitances. Certain image sensors employ decoders for row addressing (such as the tracking window example, given above), while serially accessed SRAMs benefit from using a shift register. Other architectures have also been proposed, such as daisy chaining bitcells for robust digital column-wise readout [Chandrakasan2006]. SRAMs often save power and improve performance by sub-dividing the arrays into banks, local wordlines, etc. Image sensors could partially adopt similar techniques at opposing sides of the array or fully adopt them at the expense of losing several pixels that could be compensated for through signal processing.

Column addressing, which is inherent to most SRAM designs, is used in some image sensors, when random access is necessary. Column-wise operations are performed on the data of both types of arrays; SRAMs perform write-driving, precharging and readout in this fashion, while imagers perform column-wise CDS and readout. The primary noise cancellation mechanism for imagers is the CDS function, while SRAMs often employ dummy columns for timing and level comparison. Both concepts provide opportunities to be adapted to the other field.

Both fields employ analog blocks, necessary for performance, accuracy and functionality. SRAMs use sense amplifiers to speed up readout and reduce bitline swing, while imagers use ADCs to create a digital readout from the analog signal measured by the pixel. Both are done either column-wise or one-per array (or bank). Both require biasing currents for proper operation. Both are major power consumers and should be timed carefully to operate only when necessary. Smart image sensors sometimes use alternative readout blocks, such as Winner Take All (WTA) circuits, when binary decisions are required rather than precise level readout. Similar uses could be applied to SRAMs used by specific applications.

Finally, both architectures employ digital control and timing blocks to administer their respective operating modes. Image sensors require precise timing of their reset and integration signals, as well as for CDS and ADC operation. SRAMs are often asynchronously self-timed, employing Address Transition Detectors (ATD) and other circuits to initiate precharge, read and write phases. Digital control logic maneuvers the components between operation modes, and often registers are used to latch read out signals. Careful design of these timing and control blocks can provide substantial power savings.

Table 1. summarizes the architectural similarities between SRAMs and Image Sensors:

Designation	SRAM Component	Imager Component
mxn Array	Bitcells	Pixels, in-pixel memory, in-pixel ADC
Row Addressing	Decoder, Row Drivers, wordline	Shift Register, Row Drivers, Row Selection lines, Reset lines
Column Addressing	Column Multiplexer, Bitlines	Readout columns, optional column decoder/multiplexer
Column-wise Operation	Precharge circuits, Write Drivers, Bitlines, Column Sense Amplifier	Sample and Hold, CDS, Column ADC
Analog circuitry	Sense Amplifiers, Biasing Circuitry	ADC, Biasing Circuitry, Bandgap Reference
Timing and Control	Digital Control, Self Timing logic, ATD, Dummy Column, Error Correction	Digital Control, Digital Timing

Table 1: Summary of Architectural Similarities between SRAM and Image Sensors

Peripheral Sharing

In the previous section, we discussed the similarities between SRAM arrays and Image Sensors. The correlation between the two types of arrays is even more inherent in systems that employ both units, working in cohesion to achieve certain functionalities. This is often the case in smart image sensor systems that use SRAM arrays to temporarily store previously read out data or results of image processing. In such cases, the similarities provide several architectural opportunities for sharing peripherals, thus resulting in a reduction of both power and area, and often a performance improvement due to the inherent synchronization between the units.

Figure 3. shows two examples of peripheral sharing. In the Figure 3(a), a column-wise shared architecture is shown. In this case, the readout columns of the pixel array are directly connected to the vertical writing and/or reading logic of the SRAM. A possible application is a smart image sensor that periodically stores spatial data in an embedded SRAM for further use or processing. In this case, the parallel readout of the image is directly routed

(through the column-wise processing, such as CDS, S/H and possibly ADC circuits) to the SRAM write drivers. SRAM operation is simplified to a one-dimensional (row) access scheme, as an entire row of data is read out from the image sensor and written in parallel. This architecture saves power and area, by simplifying or even eliminating the column addressing circuitry, integrating the timing and control signals of the two arrays, and even providing opportunity for replacing the SRAM's row decoder with a much smaller and less power hungry shift register. Careful design can further reduce the digital and analog blocks by creating control signals and biases appropriate for both arrays.

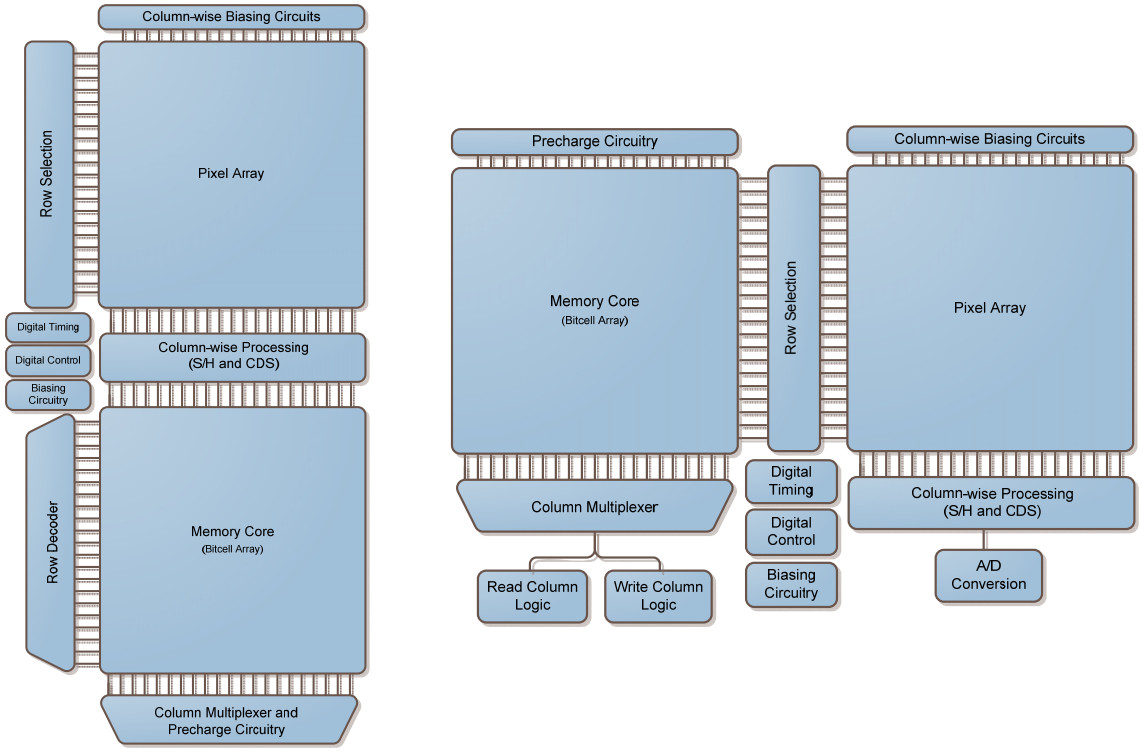

Figure 3. Two examples of peripheral sharing between SRAM and Imager arrays.

(a) Column-wise peripheral sharing. (b) Row-wise peripheral sharing

Figure 3(b) shows a possible row-wise approach to peripheral sharing. In this architecture, the two arrays are placed on a horizontal axis, enabling the distribution of row addressing signals via a mutual row selection block. One example would place a shift register in between the two arrays, asserting the reset and row selection lines of the imager in coordination with the wordlines of the SRAM, according to a predefined timing scheme. This method of SRAM addressing could be used in a serially accessed memory working in coordination with the adjacent imager. Certain applications would allow a further reduction in peripherals (saving both power and area), by integrating the column addressing blocks of the two arrays. Digital timing and control blocks could again produce common signals and analog blocks could be designed to use similar biasing levels, further integrating the two systems.

Several other peripheral sharing architectures and techniques could be proposed, depending on the application, the relationship between the smart imager and the SRAM and the operating profile of the system. Such peripheral sharing doesn't necessarily have to include complete integration between the two arrays. For example, a

significant reduction in area could be achieved by using a single bandgap reference block for a standard imager and an SRAM array on the same die, even if they are independent of each other.

These architectural opportunities should be taken into consideration when developing a system that uses both types of blocks, as the saving in power and area, as well as the prospect of performance enhancement, can be considerable. The following section gives a practical implementation example of such a system.

Implementation Example: An Improved Adaptive Bulk Biasing Control (AB²C) System

In the previous sections, we argued that image sensors and memory arrays have many common features and that power reduction techniques, developed for one field, could be adapted for the other. In addition, we proposed opportunities for peripheral sharing in systems, such as smart image sensors, that include both pixel arrays and embedded SRAM arrays. In this section, we will present an example of a system, developed by our group, that utilizes both approaches for power and area reduction, as well as performance optimization.

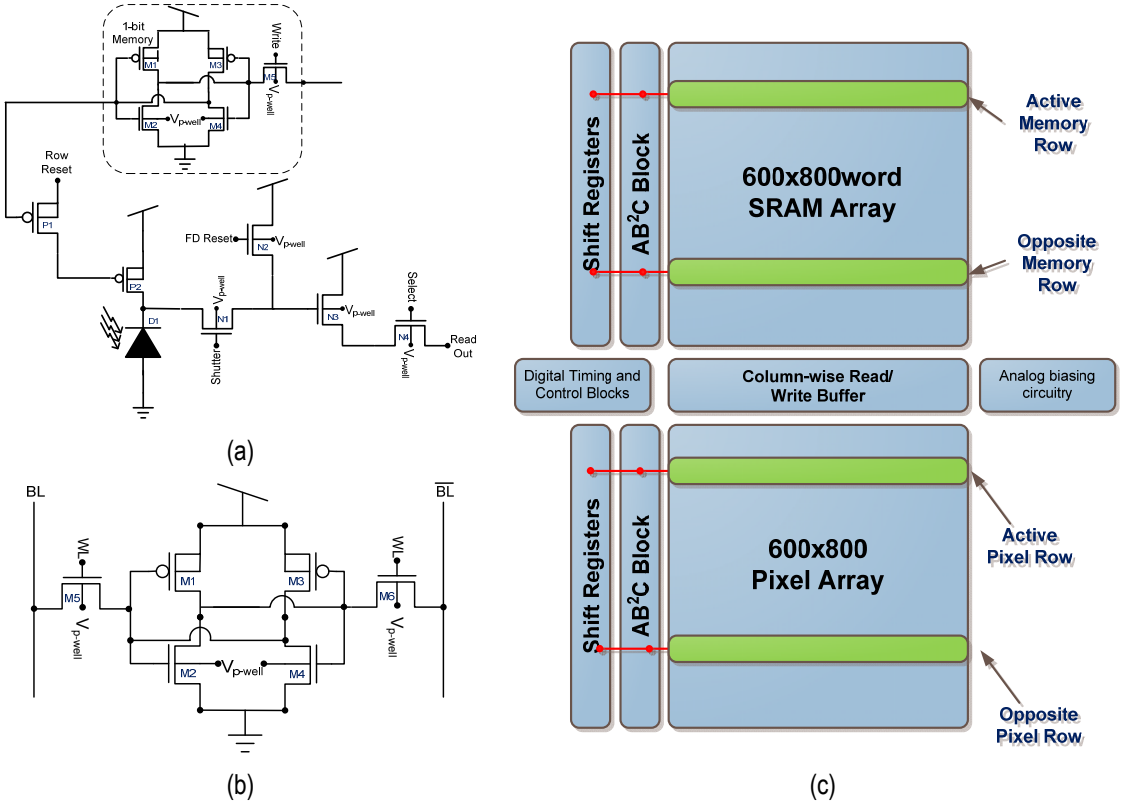

Figure 4. Architecture and basic circuits for Improved AB²C System.

(a) Schematic of Smart Pixel (b) Schematic of SRAM Bitcell (c) Full system architecture

The Adaptive Bulk Biasing Control (AB²C) approach to leakage reduction in image sensors was originally proposed by Fish, et. al. [Fish2007]. This system took advantage of the serial row access scheme, inherent to the majority of image sensors, for the application of a gradually changing body biasing to reduce the leakage in image sensors during the long integration periods. It can be shown that the slow voltage gradient applied to the bulk of a given row requires less power and causes less spatial noise than a standard pulsed approach. The

system applies the full Reversed Body Bias (RBB) to the rows farthest away from the selected (i.e. reset or readout) row, and no RBB (or potentially a performance enhancing Forward Body Bias) to the selected row.

An improved AB^{2}C system [Teman2009] implements the original concept on a smart image sensor employing an embedded memory. Figure 4(a) shows the pixel circuit implemented in the smart image sensor employing an in-pixel memory bit. The serial access scheme of the smart imager includes a periodic partial readout of the pixel level, and according to the illumination level, data is written to both the in-pixel memory bit and the embedded SRAM array. After the full integration time, the final pixel level is read out along with the data stored at the associated SRAM address. This system provides opportunities for both row-wise and column-wise peripheral sharing, due to the synchronized serial operation of the image sensor with its associated SRAM addresses. A column-wise approach was chosen, as the parallel propagation of the column data to and from the SRAM proved to be more dense.

Implementation of the adaptive bulk biasing approach for leakage reduction in the SRAM was enabled by the serial access operation, inherent to the system. A twin-well was used to separately bias the bulks of each row of nMOS transistors, as the pMOS body biasing in deep submicron technologies (a standard 90nm TSMC process was used) is inefficient. The SRAM bitcell schematic is shown in Figure 4(b). The body nodes of the nMOS transistors was connected to the AB^{2}C circuit, driven by the row addressing shift register, used to serially access the array.

The full architecture for the Improved AB^{2}C system is shown in Figure 4(c). The column-wise setup enabled parallel writing of the image sensor readout values directly into the selected SRAM word below it, and subsequent readout of the SRAM value along with the final pixel value after integration. Similar row addressing blocks were used for both arrays, comprising shift registers for horizontally wired signals (reset, row select, wordlines) and AB^{2}C circuits. These circuits include a network of resistors with connections to the bulks of rows between them. The resistor network is biased with a voltage running between the active row and the opposite row (i.e. the row farthest away from the active row), thus creating a gradual voltage drop on the bulks of adjacent rows. The bias point is switched along with the row selection shift register, causing a small charge/discharge of the row bulk capacitance, with a minimal energy penalty. The row selection blocks (including AB^{2}C circuitry) could be shared between the two arrays, pending routing options, further saving area and power.

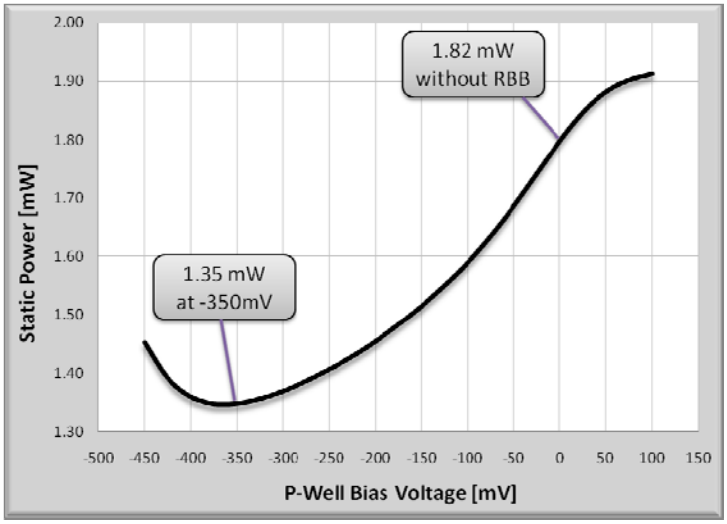

Figure 5: Static power consumption at various body biasing levels for the presented smart image sensor with embedded SRAM employing an AB^{2}C biasing scheme.

The static power reduction achieved with the application of the AB^{2}C architecture is plotted in Figure 5 for the presented system implemented in a standard TSMC 90nm CMOS process. The minimum energy point was achieved with a reverse biasing voltage of 350mV. A higher RBB results in higher power dissipation of the AB^{2}C blocks, while a lower RBB results in more pixel/bitcell leakage power. This results in a 26% power reduction as compared to the same system without the biasing voltage or the AB^{2}C power, as seen at the 0V point on the figure. This reduction improves with array sizes, and is even more effective at older technologies with a higher supply voltage, often used for image sensor implementation.

Conclusions and Further Research

A novel approach to power reduction in VLSI arrays was presented. The architectures of two types of arrays, image sensors and SRAM arrays were described. Sources of power consumption were noted for each array type, and some common techniques for power reduction were shown. It was contended that the similarities between the array types provide many opportunities for adaptation of methods and techniques for power reduction and optimization between the two. A number of architectural concepts based on peripheral sharing were suggested for systems employing both types of arrays. Finally, an example of a system that implements both approaches (method adaptation and peripheral sharing) was presented. The example showed an AB^{2}C scheme that was originally developed for image sensors and was implemented on an SRAM array, as well, providing a substantial static power reduction for the entire system. The image sensor and SRAM array were connected in a column-wise scheme, further saving both area and power, while optimizing the operation process.

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