VHDL-MODELING OF A GAS LASER'S GAS DISCHARGE CIRCUIT

Nataliya Golian, Vera Golian, Olga Kalynychenko

***Abstract**: Usage of modeling for construction of laser installations today is actual in connection with automation of manufacture. The automated designing is used at forecasting behavior of modeled objects That is why at the certain stage of development CAD there was a necessity of creation of standardized language of the description of the equipment, one of which is VHDL. It allows to describe the behavior of digital circuits, as well as to perform and also to spend the hierarchical functional-structural description of the big integrated systems and at the same time has all signs of the programming language of high level – allows to create the types of the data, has a wide set of arithmetic and logic operations. The paper suggests synthesis of a VHDL – model of a gas laser gas-discharge circuit efficiently distributing RTL- circuits to create a new list of connections with a minimum number of components. Models of GDC lasers consist of three subtasks: a logic conclusion, optimization received RTL structures and its distribution on structural elements technology mapping*

***Keywords**: model of a gas laser, gas-discharge circuit, VHDL – model, gas discharge circuit*

***ACM Classification Keywords**: C.4 Performance of systems - Modeling techniques*

Introduction

Designing long scale integrations (LSIC) is impossible without the availability of powerful CADs. Developing CAD means of a gas laser gas-discharge circuit is critical problem.

Modern CAD have is functional-block structure, in accordance with which different stages of a design cycle are performed by corresponding subsystems. This has led to the appearance of individual systems frequently developed by a variety of manufacturers majoring in the , performance only one of stages (for example, a synthesis stage).

In addition, CAD is becoming a through one: all the design stages – microcircuits modeling, synthesis, implementation and programming are carried out in a common medium. [Ovezgeldyev, 2002]

It permits to verity devices at all the design stages, which enables to reduce the probability of emergence of errors. Therefore at a definite stage of CAD development there appeared a need for developing standardized – languages of equipment description, one of which is VHDL.

VHDL is a powerful language which allows to describe the behavior of digital circuits, as well as to perform and also to spend the hierarchical functional-structural description of the big integrated systems and at the same time has all signs of the programming language of high level – allows to create the types of the data, has a wide set of arithmetic and logic operations [Golian, 2003].

Designing of a gas laser gas-discharge circuit

In designing the following parameters must be provided:

- the pressure at the gas discharge circuit (GDC) input shell of 14 mm (base = K). There is exist a possibility to set value of K within 3... 15. This parameter will define a range of representation of size of pressure value $0 \le A \le K - 1$ and the number of bits at the GDC output (to must be sufficient to place the greatest number Amax =) K – 1;
- the GDC structure must change depending upon the mentioned parameters.

Consider the generalized GDC structure. The device interface is shown in Fig 1.

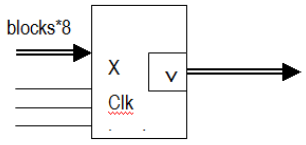

Figure 1. Tthe device Interface

The description of ports is resulted the table 1.

Table 1. Description of ports

X ((blocks*8-1): 0)	input	Blocks – 8 digit; data bus through which loading code takes place
Reset	input	Signal with an actual bag level, providing the reset of discharge counter an accumulator and on output buffer register
Clk	input	Synchronizing signal (active leading edge)
Load	input	Signal providing the selection of a source of input data in operational automatus block as well as the rest of a accumulator to at the beginning of each new conversion
Y(47:0)	output	48 – digit data bus though which the GDC code is rolled out

Purpose and possibilities of synthesis GDC a VHDL-model

Problem of the synthesis of system is effective distribution of the RTL-circuit with the aim of creating a new list of connections with a minimum number of circuit components used. Each component of the new list will correspond to the physical hardware block in the FPGA (elements of configured logical blocks, anticipated carry logic).

Hierarchical designs are synthesized in an ascending regime when components of the lower level are synthesized up to those of a upper level.

The device model in the language of describing VHDL equipment must be adapted for synthesis and implementation on FPGA chip of the XILINX firm.

The problem of a choosing on hardware platform is of great important for the designer. The right choice will enable:

- to reduce material cost in the implementation of the device ;
- to attain optimum functioning and speed of operation .

According to the technical requirement the GDC model must be adapted for synthesis and implementation on the FPGA of the Xilinx firm. In choosing FPLD of most of the focus is on the relation between its cost and productivity. Besides it is necessary to take into account the crystal which will be occupied by the synthesized device. [Cardoso, 2003]

FPGA (Field Programmable Gate Arrays) were first developed by the Xilinx firm in 1985. Tuning a FPGA on the specified functioning is carried out each time before the start of its operation. The required setup program is preliminary recorded in ROM (RAM).

Loading information from ROM and FPGA automated initialization after turning on power supply (for this the FPGA contains the required logic circuits). One can also carry out FPGA tuning under the control of a microprocessor or microcontroller.

FPGA has typical structure of a gate array. Fig. 2 shows the Xilinx firms FPGA - Spartan II (XC2S30 model). The Xilinx firms EPLD of FPGA type are implemented on the base SRAM in accordance with MOS technology. They are characterized by high flexibility of structure and abundance on a crystal of triggers. Thus the logic is realized by means of a matrix so-called LUT - tables (Look Up Table), and internal interconnections - by means of the branched out hierarchy of the metal lines switched by special high-speed transistors.

The considerable cost of FPGA micro circuits with built in RAM in comparison with an embedded RAM in comparison to that of custom microcircuits restricts the use of FPGA for manufacturing pilot models or small-scale production. This defect of the FPGA has been eliminated by firm Xilinx firm by manufacturing a new series of microcircuits FPGA - series Spartan and Spartan-II. The parameters of the Spartan II (model XC2S30) are given in table 2 (logic cells, the number of system gates, CLB array dimensions, CLB number etc.).

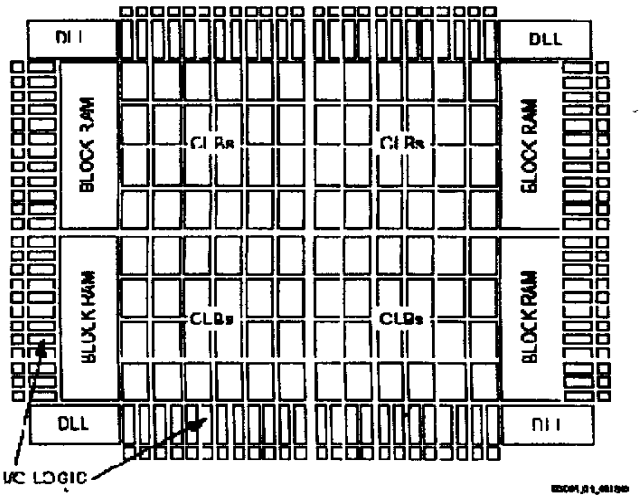

Figure 2. Structure of Spartan-II chip

Table 2. Parameters of FPGA Spartan-II family

Logic Cells	System Gates (Logic and RAM)	CLB Array (CxR)	Total CLBs	Maximum Available User I/O	Total Distributed RAM Bits	Total Block RAM Bits
972	30000	12x18	216	132	13824	24K

The FPGA Spartan-II family has a record low cost per a gate on the density of packing up to 200 thousand gates. In a crystal there is four blocks of the RAM each having 4KBits, besides it in possible to implement 16 bits of memory on each 4 input functional generator. The Spartan-II device combine lines of flexible regular architecture which include a CLB matrix surrounded by programmable input – output blocks inter connected by a hierarchy of high – speed, multi – sided resources by a history of high-speed, multi – sided recourses of interconnections.

The Spartan-II devices have high productiveness in comparison to the previous FPGA families. The designs can operate at a system synchronization frequency of up 200 MHz, including input/conclusion blocks (Input/Output-I/O).

Besides, Spartan-II chips are distinct in a large variety of advantages, namely:

- relatively low of crystal cost;
- big chip dimensions (up to 200 000 system gates);
- high speed of operation.

The Spartan-II, shown in fig. 2, covers configured logic blocks (configurable logic blocks - CLBs) and input-output blocks (IOBs). CLB blocks serve for creation of functional logic elements, and blocks IOBs create on interface between microchip contacts and CLBs.

Configurable logic block (CLB). A logic cell (Logic Cell – LC) is the basic structural elements of a CLB. The logic element includes 4-input functional generator, high – speed carry logic and a memory element. The output of functional generator is connected to the output logic of the CLB-block and D-input of a trigger. Each CLB in the

Spartan-II series contains four logic cells organized in the form of two identical slices. Fig.3 shows one slice in more details.

In addition to four base logic cells, the CLB-block of series Spartan-II contains logic that allows to combine resources of functional generators for realization of functions from five or six inputs.

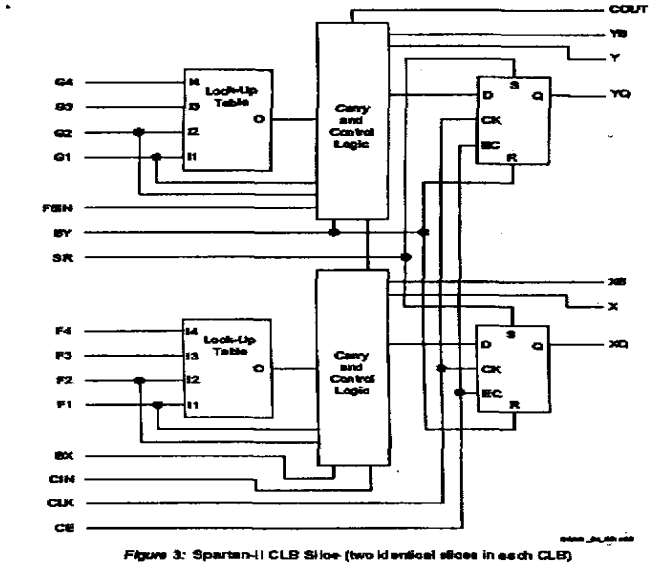

Figure 3. Vi cell of FPGA Spartan-II

Look-Up Tables (LUT). The functional generators are implemented in the form of 4 - input functional tables (LUT). In addition to the use as functional generators, each LUT-element can also be used as synchronous RAM of 16x1 bit dimension. Moreover is more, out of two LUT-elements within one slice one can implement either synchronous RAM of 16x2 a bat or 32x1 bit dimension or two-port synchronous RAM of 16x1 bit dimensions.

A 16-bit shift chain, which perfectly fits to capture high-speed or both data flows, can be implemented on the basis of a Spartan-II microcircuit LUT-element. The regime can also be used to story data in such appendices as digital signal processing (Digital Signal Processing - DSP).

Memory elements (ME). MEs in each slice of a Spartan-II CLB can be configured as dynamic triggers (sensitive to wave - front) or doors sensitive to signal strength. A trigger D-input can be controlled either from a functional generator within the same slicer of a CLB, or directly the inputs of this slice.

Additional logic in a CLB. A F5 multiplexer in each slice combines the outputs of a converter.. This combination enables to implement any function of 5 variables or some functions of up to nine variables. In the same way a F6 multiplexer combines the outputs of all four output in CLB. They allows to implement any function of 6 variables as some functions of to 19 variables. Each CLB has four direct paths. These paths provide additional data input lines or additional routing which allows to save logic resources.

Arithmetic logic. Special transfer logic provided an opportunity of fast transfer in implementing arithmetic functions. The Spartan-II CLB supports two individual transfer chains, one for each CLB slice. The dimension of transfer chains are two bits per a CLB.

RAM block. A special block memory is embedded in the FPGA Spartan-II. It is created in addition to a distributed small - capacity (Select RAM) memory, implemented on functional tables (Look Up Table RAM - LUTRAM).

Choice of instruments. The firm Synplicity software product Synplify 7,0 is chosen for synthesizing the design as it has following advantages programs of other manufacturers:

- high speed of synthesis;
- visual representation of the results of synthesis;
- availability of libraries for the present- day element base of the biggest world manufacturers.

The design analyzed is synthesized into a library repertoire of primitives.

The list of connections after the stage of a logic output is made out of abstract logic elements, such as accumulators, counters, multipliers, receivers as well as gates and synchronous triggers. These circuit elements must be further placed in structural components of the EPLD technology used. This process also is called as technological distribution on FPGA-chip.

In order to make sure that the system agrees with the specification, it is necessary to verify, i.e. to model it (Fig. 4)

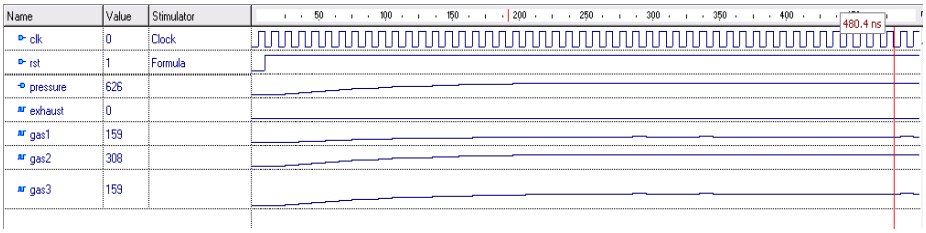

Figure 4. Result of modeling a gas –discharging

Conclusion

The possibilities of the syntheses VHDL - models of GDC lasers, which will consist of three subtasks: a logic conclusion, optimization received RTL structures and its distribution on structural elements technology mapping.

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