SELF-ASSEMBLY PROCESS FOR INTEGRATED CIRCUITS BASED ON CARBON NANOTUBES USING MICROFLUIDIC DEVICES

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***Abstract**: New methods are needed to create integrated circuits which are able to overcome the inherent problems in the miniaturization process. These problems are mainly technological and economical; photolithography is limited and the expensive building respectively. This paper proposes the basis for a new manufacturing process of nanotechnological circuits based on semiconducting carbon nanotubes that work as FET (Field Effect Transistor) and metallic carbon nanotubes that work as nanowires. This process is based on the assembly of DNA tiles and lattices that guide the placement of carbon nanotubes to build electronic circuits. The process takes place in a microfluidic device within its chambers. Building blocks are created based on NAND logic gates. These building blocks are enabled to assemble AND, OR and NOT logic gates. The process of assembling a XOR logic gate is explained, demonstrating how to apply the process in a concrete case.*

***Keywords**: Carbon nanotubes, DNA lattice, FET, Microfluidic devices, Self-assembly process.*

***ACM Classification Keywords:** B.7.1 Types and Design Styles – Advanced technologies*

Introduction

With the technologies used today, Moore's law is going to touch the ceiling and will not be possible to further reduce the size of transistors and to double the number of them per unit area. This affirmation conduces at the search of new materials and paradigms for the construction of computing circuits Current methods of manufacturing integrated circuits have absolute control of the assembly of components but there are economic and technological limitations (factories are too expensive and photolithography has precision limitations, respectively).

Nanotechnology allows working on the atomic scale and the main advantage about this is the reduction of the circuit size. But nanotechnology has to deal with two issues for building reliable circuits: manufacturing defects and faults. Manufacturing defects are due to the imperfect fabrication process inherent to nanoscale properties. A fault is an incorrect state of the system due to manufacturing defects, component failures, environmental conditions etc. Faults can be permanent, due to system defects; intermittent, faults appear periodically; transient, due to temporary environmental conditions. A system with defect tolerance is able to operate correctly in the presence of manufacturing defects. A system with fault tolerance is able to operate correctly in the presence of permanent, intermittent or transient faults. The most used method to achieve defect tolerance and fault tolerance is components redundancy. Moreover, defect tolerance and fault tolerance can be achieved at several levels: physical level, architectural level and application level [Graham et al., 2004].

This paper presents a proposal of a new approach for nanotechnological circuit fabrication in a controlled manner without going into depth on technological details on nanotechnology and microfluidic devices. The proposed approach uses a microfluidic device to build an electronic circuit based on carbon nanotubes that are self-assembled through DNA tiles. The idea is based on the works about DNA lattices assembled within microfluidic devices and works about how to use DNA tiles and lattices to assemble carbon nanotubes to build circuits. In a first state of the process, building blocks are assembled based on NAND gates within the microfluidic device

chambers. This NAND logic gates are supposed to be the same as the developed ones in other works. This is the base to build any circuit possible, memories, ALU etc.

This paper is structured in the next manner: section 2 provides background about using DNA lattices for manipulating and self-assembling carbon nanotubes and using microfluidic circuits for DNA lattices assembly; section 3 sets out the components and operation of the proposed micro fluidic device; section 4 to section 6 explains in detail the self-assembly process; section 7 shows an example of the process based on XOR logic gate; section 8 explains some generalization about the process and the last section shows conclusions and future work.

Background

L. Adleman was the first researcher in to demonstrate the computing capacities of DNA based on strands hybridization. In [Adleman, 1994] is showed the resolution of a simple Hamiltonian path problem, a NP-Complete problem, with DNA strands. After Adleman's works, Lipton was solved a simple SAT problem, a NP-Complete problem using DNA as [Lipton, 1998] and in [Winfree et al., 1996] was shown the universal computing capacity of self-assembled DNA strands.

This complementarity of bases also allows creating tiles of DNA strands to be assembled in a lattice, such as scaffolded DNA Origami [Rothemund, 2006]. In [Dwyer et al., 2004b] is showed how to create self-assembling computer circuits with DNA facilitating the use of other components for the computing itself, for it makes use of a decoupled array multi-processor (DAMP), similar to a single-design instruction, multiple-data (SIMD).

In these papers [Keren et al., 2003], [Dwyer, 2002], [Dwyer et al., 2004a], [Maune et al., 2009], [Patwardhan et al., 2004] is showed how to use DNA lattices in combination with carbon nanotubes as field effect transistors (FET) to build computer circuits. Carbon nanotubes can be used as FET due to the ability of these semiconducting nanotubes to be modulated applying a gate voltage and the ability to separate metallic nanotubes from semiconducting nanotubes and controlling the length of individual nanotubes.

Specifically, in [Maune et al., 2009] is observed the assembly process for a carbon nanotube into a DNA lattice, which consists of:

1. Designing a DNA strand with one end, the 5 'end, with forty T bases, which will assemble the carbon nanotube, and 20 bases with a certain combination, of which the 15 bases that follow the 40 T bases will be hybridized with their complementary base, the toe, freeing five bases at the other end, the 3 '.
2. The lattice has chains of DNA that are complementary to the 20 bases completely different from the 40 Ts. By having five free bases, the attraction of the lattice, fully complementary, is more favorable thermodynamically than the 15 bases toe, so that in the end, the chain that carries the carbon nanotube hybridizes with the lattice.

In [Dwyer et al., 2004a] and [Patwardhan et al., 2004] are proposed the build of a full adder and a SR-latch through DNA lattices and carbon nanotubes NAND gates They used two types of carbon nanotubes, attached in a perpendicular way: the metallic carbon nanotube acts as a gate, and the semiconducting carbon nanotube acts as channel in a CFNET. The nanotubes used as wires are attached to each side of each cavity in the tile. This proposed process has limitations in the number of FETs (100x100), in the size and complexity of the circuit. For this reason, these authors warn the necessity of a modular design to allow building larger circuits.

In this sense, the process of creating DNA lattices can be improved via microfluidic circuits. A microfluidic circuit is a configuration of microscale fluidic components such as microchannels, individually addressable valves and chambers through which fluid is allowed to flow [Dutta, 2008]. Microfluidic circuits can be represented as electrical circuits and have components as fluidic resistors, capacitors, inductors and transistors. Therefore, microfluidic circuits can be characterized by fluidic resistance, fluidic inductance, fluidic capacitance, fluidic transistors, fluidic

amplifiers and fluidic logic. There are two main types of microfluidic circuits: fluidic circuits for pressure-driven flow and fluidic circuits for electrokinetically driven flow. Fluidic circuits for pressure-driven flow are based on fluid resistance. In fluidic circuits for electrokinetically driven flow, an ionized liquid can be forced to move in a dielectric capillary or microchannel under the action of an externally applied electric field [Dutta, 2008]. An interesting advantage is that flow rate can be controlled very precisely using an externally applied electric field.

In [Somei et al., 2006] are showed the difficulties in assembly DNA lattices due to aspects as the hardness of maintaining the concentrations of monomers or the 1% in errors of assembling . The solution proposed is the use of a microfluidic device for the assembling process of the DNA lattice. This architecture consists of:

a) A service port where the DNA sample solution is applied by pipetting.

b) A reaction chamber where the self-assembly DNA tile participates under controlled temperature.

c) A capillary pump which generates suction force to pull the next solution from the service port.

The different tiles are assembled in the chambers. The chambers are connected in a way that tiles are assembled in the desired manner in other chambers. The process is totally controlled due to the microfluidic device.

Self-assembly process using microfluidic devices: description

The start point after Somei's work would be to use a similar microfluidic circuit [Somei et al., 2006]. This proposed circuit self assembles the tiles with carbon nanotubes, within the chambers of the device. Each chamber can to assemble different logic gates and wires. The microfluidic device used is a fluidic circuit for pressure-driven flow.

In order to manufacture specific circuits, able to self-assemble, is necessary assembled different logic gates as well as create different tiles for the same logic gates, varying the type of input and output for this gates. T Based on NAND gate was proposed in [Dwyer et al., 2004] and using the logic gate NAND, our microfluidic circuit will have three basic phases in the self-assembly of logic gates:

1. NAND gates are assembled in order to build the rest of the required logic gates.
2. The logic gates based on the NAND gates are built.
3. Adapters are built to connect the assembled gates. This last phase depends on the circuit to be build.

The process depicted is incomplete because the assembled circuit is not ready to be used as an electronic device. The assembled circuit needs a procedure like the described in [Keren et al., 2003] for CFNETs.

It is assumed that the component to be built has several input signals. These signals are shared by every logic gate within the component and one or more output signals. It is considered a component: anything is assembled within a chamber.

It is necessary for the first phase, to define several and different DNA strands, which are markers of input and output signals. These markers point out the gates which are their inputs and outputs and they guide the assembly process within the chambers. The used strands are defined as follows:

- I_i is a strand that indicates the signal i is an input of the component corresponding to the logic gate.

- O_{ij} is a strand that indicates the output of the logic gate with input signal *i* and input signal *j*.

- $I_{O_{ij}}$ is a strand that indicates the input of the logic gate is the output O_{ij} of another logic gate.

The chambers where the components are assembled are denominated $C_{component}$, where *component* is the name of the component assembled within the chamber.

The adapters, components are denominated $A_{input/output_i}$, where $input$ is the name of the component whose output is the input of the adapter and $output_i$ is the name of the component whose input i is the output of the adapter.

The process to build the logic gates OR, AND and NOT through a microfluidic device from NAND gate are presented. In addition, an example of a new assembled logic gate based on the created logic gates, an XOR, is illustrated. In this process, only two input signals to the components are considered.

Phase 1: building blocks for the assembly of OR, AND and NOT logic gates.

In this first phase, in the microfluidic circuit is necessary to have the same number of chambers and components. The subject of this phase is to define an inverter that is showing in the next figure. Two types of inverters are needed: NOT_{11} and NOT_{22}. NOT_{11} has input signal 1 as input and NOT_{22} has input signal 2 as input. Both components are showed in the figure 1.

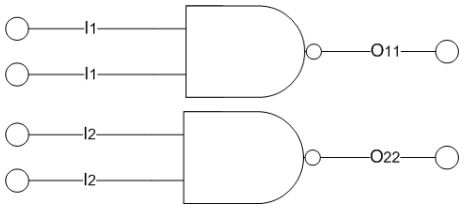

Figure 1. NOT logic gates

The building blocks for assembling OR logic gate are the components NOT_{11} and NOT_{22} and a new gate, a NAND gate, designated by $NAND_{11\_22}$ which has as inputs the outputs of NOT_{11} and NOT_{22}. This new NAND gate is showed in the figure below.

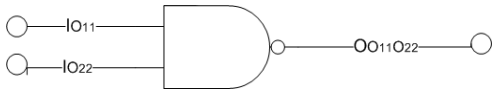

Figure 2. OR gate components

The building blocks for assembling AND logic gate are two NAND gates: $NAND_{12}$ and $NAND_{12\_12}$. The gate $NAND_{12}$ has as input signals the signal 1 and signal 2 of the circuit. $NAND_{12\_12}$. has as inputs the outputs of two $NAND_{12}$. The AND component is showed in figure 3.

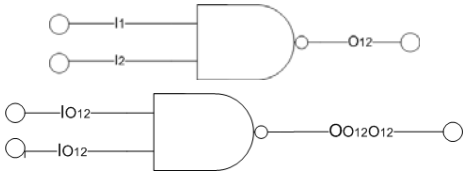

Figure 3. AND gate components

Once it is well known how to build the components, 5 chambers are necessary to assemble the 5 building blocks: $C_{NOT_{11}}$, $C_{NOT_{22}}$, $C_{NAND_{11\_22}}$, $C_{NAND_{12}}$, $C_{NAND_{11\_22}}$ and 7 different DNA strands are necessary to associate to each input and output used:

- I_1 , I_2 , O_{11} , O_{22} , O_{12} , $O_{O_{11}O_{22}}$ and $O_{O_{12}O_{12}}$ have their own DNA strand for the subsequent assembly with the other components.

- $I_{o_{11}}$ has associated the complementary strand of O_{11} .
- $I_{o_{22}}$ has associated the complementary strand of O_{22} .
- $I_{o_{12}}$ has associated the complementary strand of O_{12} .

The DNA strands and the carbon nanotubes solution is applied by pipetting the corresponding service ports. The assembly process is realized within the chambers.

Phase 2: Assembling OR and AND gates.

In this phase, a new solution is applied by pipetting the corresponding service ports. This causes the new assembled components flowing from their chambers to the next chambers. Then, a new assembly process is generated. This process is responsible of the building the OR and AND gates.

To assemble the OR gates, is necessary a chamber to combine the products of $C_{NOT_{11}}$, $C_{NOT_{22}}$, $C_{NAND_{11\_22}}$ chambers. OR gate is shown in figure 4.

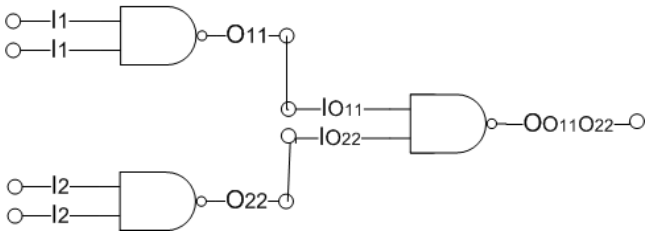

Figure 4. OR logic gate

To assemble the AND gates, is necessary a chamber to combine the products of $C_{NOT_{12}}$, $C_{NAND_{12\_12}}$ chambers. To obtain a number of AND gates, are necessary the same number of $NAND_{12\_12}$ components and the double of $NAND_{12}$ components. AND gate is shown in figure 5.

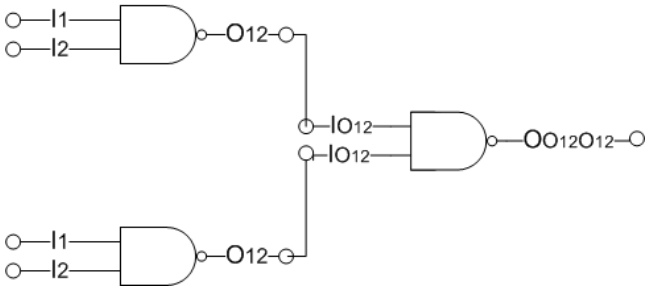

Figure 5. AND logic gate

Once it is well known how to build the components, 2 chambers are needed to assemble the 2 logic gates: C_{OR} , C_{AND} . At this moment of the assembly procedure, 7 chambers are necessary.

Phase 3: Creating adapters between logic gates

At this point, it is necessary a new type of component: the adapter. The adapter connects the outputs of the logic gates with the inputs of another logic gates. This component, which is a tile, is composed by the complementary strands of the outputs of the logic gates and the complementary strands of the inputs of the gates to be connected. This component is an interface between logic gates. It could be a signal amplifier, if carbon nanotubes as FETs are assembled within the tile. The adapters could be used to switch on or switch off parts of the circuit.

An example: XOR logic gate

Based on the components resulting from phases 1 and 2, and the adapters were described in phase 3, we build a XOR logic gate. The input signals of the component are the input signal 1 and the input signal 2.

To build a XOR gate we need two NOT gates, two AND gates, one OR gate and the following adapters:

- An adapter whose input is the complementary DNA strand of the output DNA strand of a component NOT_{11} and whose output is the complementary DNA strand of the first input of an AND gate. It is denominated A_{NOT_{11}/AND_1} .

- An adapter whose input is the complementary DNA strand of the output DNA strand of a component NOT_{22} and whose output is the complementary DNA strand of the second input of an AND gate. It is denominated A_{NOT_{22}/AND_2} .

- An adapter whose input is the complementary DNA strand of the output DNA strand of an AND gate and whose output is the complementary DNA strand of the first input of an OR gate. It is denominated A_{AND/OR_1} .

- An adapter whose input is the complementary DNA strand of the output DNA strand of an AND gate and whose output is the complementary DNA strand of the second input of an OR gate. It is denominated A_{AND/OR_2} .

For each adapter, two chambers are necessary. The first chamber is necessary to assemble the adapter with the gate whose output is the input of the adapter. The other chamber assembles the adapter with the gate whose input is the output of the adapter.. This is the process needed to avoid undesirable hybridization between logic gates whose input is the output of a logic gate of the same type. This example relies in 8 new chambers and the total of the chambers is 15.

The assembly process for the XOR logic gate is composed by the next phases:

1. Assembly of adapters of the AND gates with their inputs:

   a) Assembling adapters A_{NOT_{11}/AND_1} with NOT_{11} components, which are products of $C_{NOT_{11}}$ chamber, within C_{A_1} chamber.

   b) Assembling adapters A_{NOT_{22}/AND_2} with NOT_{22} components, which are products of $C_{NOT_{22}}$ chamber, within C_{A_2} chamber.

2. Assembly of adapters of the AND gates with their outputs:

a) Assembling adapters A_{NOT_{11}/AND_1}, which are products of C_{A_1} chamber, with input 1 of AND gates which are products of C_{AND} chamber, within C_{AND_1} chamber.

b) Assembling adapters A_{NOT_{22}/AND_2}, which are products of C_{A_2} chamber, with input 2 of AND gates, which are product s of C_{AND} chamber, within C_{AND_2} chamber.

This phase needs a dispatcher after the chamber C_{AND} having the same probability of dispatching AND gates to C_{AND_1} and C_{AND_2} chambers.

3. Assembly of adapters of the OR gates with their inputs:

a) Assembling adapters A_{AND/OR_1} with AND gates, which are products of C_{AND_1} chamber, within C_{A_3} chamber.

b) Assembling adapters A_{AND/OR_2} with AND gates, which are products of C_{AND_2} chamber, within C_{A_4} chamber.

4. Assembly of adapters A_{AND/OR_1}, which are products of C_{A_3} chamber, with input 1 of OR gates, which are products of C_{OR} chamber, within C_{OR_1} chamber.

5. Assembly of adapters A_{AND/OR_2}, which are products of C_{A_4} chamber, with input 2 of OR gates, which are products of C_{OR_1} chamber, within C_{OR_2} chamber.

The desired components, XOR logic gate, are within C_{OR_2} chamber.

Generalizations of the self-assembly process

The process proposed in this paper has only two input signals. The number of DNA strands and chambers for the process depicted are for two input signals. This process can be generalized for more input signals. Different DNA strands are used for each input and output signals of the building blocks. The next formula shows the upper bound of the number of different chains that are necessary depending on the number of signals, denominated as N.

$$2N + 3\binom{N}{2} \simeq O(N^2)$$

Figure 6. Upper bound of DNA strands

Where:

$2N$ is the number of input signals plus number of outputs of the inverters for each signal;

$\binom{N}{2}$ is the number of all the possible outputs of the OR building blocks;

$2\binom{N}{2}$ is the number of outputs of the AND building blocks.

The upper bound of the number of chambers needed for phases 1 and 2 depends on the number of input signals. The formula is illustrated below (N as the number of signals):

$$N + 3\binom{N}{2} \simeq O(N^2)$$

Figure 7. Upper bound of chambers

Where:

N is the number of inverters for each signal;

$\binom{N}{2}$ is the number of all the possible OR building blocks;

$2\binom{N}{2}$ is the number of all the possible AND building blocks.

Both, the upper bound of the number of DNA strands and the upper bound of the number of chambers have a quadratic growth respect to the number of input signals.

Conclusions and Future work

In this paper it has been shown how to build circuits with carbon nanotubes as field effect transistors (FET) in a self-assembly way using DNA strands. First, the tiles are assembled and later the lattices are compound. In this process is proposed the use of microfluidic circuits for the assembly procedure. The assembly procedure starts with the creation of building blocks based on NAND logic gates. These building blocks are enable to assemble AND, OR and NOT gates. In addition, an example of building a simple component with a XOR gate was illustrated.

In particular, for the hybridization of inputs and outputs are only needed seven different chains and their complementary DNA strands and only eight chambers to create gates AND, OR and NOT. The upper bound of the number of different DNA strands and the upper bound of the number of chambers for phases 1 and 2 of the assembly process have a quadratic growth respect to the number of input signals.

The amount of carbon nanotubes and DNA strands needed to assemble certain number of components is unknown because the results of the assembly process are probabilistic. This means that the exact number of components cannot be guaranteed but a lower bound for this amount can be obtained. This lower bound is the number of assembled components desired. Therefore, this implies to know the performance of reactions within the chambers. In this sense, simulations are needed for testing the performance of the microfluidic device proposed and the circuit manufactured within the microfluidic device. As well, is necessary the simulation of the components and circuits assembled in the process. The results can be analyzed to set the impact of the insertion of the adapters into the performance of the circuit.

Now, the limits of size and complexity of the assembled circuits can be related to the limitations in design and manufacturing of the microfluidic device.

Finally, it is possible to add more functionality to the adapters. They could be used as part of a defect and fault tolerance system, based on Multiplexing NAND for the assembled circuit.

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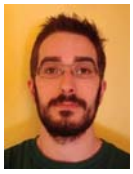

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